DERWENT-ACC-NO: 2000-079665

DERWENT-WEEK: 200007

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TITLE: Memory accessing circuit in digital signal processor - includes shared memory addresses generator which generates shared memory, so that input-output of register value is performed through main bus

PRIORITY-DATA: 1998JP-0126990 (May 11, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 11328010 A	November 30, 1999	N/A	004	G06F 012/06

INT-CL (IPC): G06F012/06

ABSTRACTED-PUB-NO: JP 11328010A

BASIC-ABSTRACT:

NOVELTY - The shared memory (8) accesses data independently through the data buses (3,4). Shared memory address generators (9,10) which generate shared memory addresses, so that input and outputs of register value is performed through the main bus (7).

USE - For memory accessing, in digital signal processor.

ADVANTAGE - Data memory access is optimized and hence reduces number of arithmetic processings involved. DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the data memory accessing circuit. (3,4) Data buses; (7) Main bus; (8) Shared memory.

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Basic Abstract Text - ABTX (3):
ADVANTAGE - Data memory access is optimized and hence reduces number of
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the block diagram of the data memory accessing circuit. (3,4) Data buses; (7) Main bus; (8) Shared memory.

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